A System Level Solution to Improve VRM Efficiency

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***Abstract*–An investigation of the synchronous buck regulator working as a Voltage regulator module (VRM) for Processor power supply applications, under light load condition is presented. VRM, a very special case of power supply belongs to switched mode power supply family. Important design specifications include low output voltage with extremely small tolerance band, high load current of large slew rates, small foot print, low cost etc. Higher operating efficiencies are desired to enable extended battery mode operation in mobile platforms in addition to reducing heat dissipation. This paper identifies the source of energy inefficiency and suggests a variable frequency approach as a cost effective system level solution, to enhance the efficiency of the converter supplying widely varying load with special emphasis to light load operation.**

I. INTRODUCTION

The power supply solutions for the new generation processors are challenging as their designs have to meet a number of constraints. Deep sub-micron technologies are used for the processor implementation to reduce the power consumption, which works with a voltage profile around 1V. Compiler algorithms are well equipped with many features to facilitate power saving in processor load cycles. Accordingly the processor architecture along with the compiler, have been designed suitably to work in different states for best exploiting energy saving features. In addition to dynamically scaling the voltage, energy consumption is kept lowest while processor is in sleep state as compared to its working in active state where it consumes highest power. For example a processor implemented in 90nm technology is expected to work with a voltage profile from 0.825 to 1.6V. Processor provides its voltage profile requirement, through a six bit voltage identification code (VID), as and when it's working state changes [1]. This code sets the reference voltage for the VRM control circuit. Moreover fast dynamic transients occur when the processor chip moves from sleep state to active mode and vice-versa. With the increasing clock frequencies, the current slew rate at the sensing point of the socket is expected to reach to 4 - 5 A/ns for server class processors as compared to the present 450 A/μs [2]. To add to this, the VLSI technology is expected to further shrink in accordance with the trend line. As a result the processor designer is likely to add more functions in the same chip area. This indicates that the processor is expected to demand large currents of the order of hundreds of Amperes, in laptop, desktop and server class machines.

The processor VRM, other DC/DC converters and the system loads are generally connected to a power selector, which selects between two input energy sources: the battery packs and the power adaptor. The voltage range of Lithium battery cell is 4.2~2.9V. A voltage range of 16.8~8.7V is created with a pack of three or four cells. The adaptor provides 19V to charge the battery. The VRM must then be designed to work with a source voltage ranging over 8.7~19V for laptop applications [3]. However in desktop applications the switched mode power supply will deliver voltage more tightly at 12V±5%. Hence the VRM will have to work with predefined source voltage variation and deliver power to processor load over its expected voltage range [4]. Other design constraints include allowable output voltage swing to be less than ±20mV for high di/dt load change, small foot print, and high efficiency. These performance requirements pose serious challenges for the VR design.

Among the topologies, multiple converters, interleaved in time phase are shown very efficient for supplying large processor current demand [5], [6]. All the phases being identical, efficiency improvements are then confined to within the topology and its control techniques. In this direction many topologies with improved control strategies have been suggested. Autotransformer version buck converters [7]-[8], self driven soft-switching techniques [9], [10], two stage architecture [3], [11], [12], single-stage multiphase version [13] etc, all group into basic synchronous buck converter derived topologies [14]. All the propositions or improvements shown are with a definite premium of extra cost or complex control. Any increase in the power efficiency during light load or idle state operation significantly contributes to extend the battery mode operation. This paper attempts to demonstrate a cost effective measure of improving efficiency in the basic buck converter topology itself under light load operation in particular.

II. CONVERTER STEADY STATE ANALYSIS

The synchronous buck converter topology in its simplest form, as shown in Fig. 1 is used for the analysis. During steady state the converter is expected to deliver lower voltage from a much larger source voltage. The control MOSFET transfers the energy from input to output and rectifier MOSFET facilitates the inductor energy freewheeling. Lower duty ratio necessitates MOSFET M2 to conduct for longer periods and hence lower ON-state resistance (R_{DS}) for MOSFET M2 can help in achieving higher efficiency. At the same time MOSFET M1 need to be fast while switching ON and OFF as its conduction time is very small. Control MOSFET M1 selected with lower Figure of Merit (FOM=R_{DS}*Q_G; Q_G is the MOSFET gate charge) is shown to be very efficient [15].

To achieve faster transient response the converter is allowed to operate in continuous current mode (CCM). During each

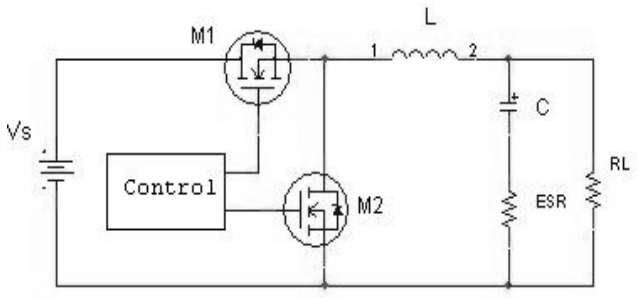

Fig.1 Synchronous rectifier buck converter [14]

switching cycle the inductor current rises from a minima, reaches to peak value, and then returns back to the same minima. The input voltage, output voltage and load current of each converter decide the current continuity of inductor, and are a part of the design specification. Hence inductor value selection becomes critical in obtaining best transient response and energy efficiency. The minimum value of inductance (L_{MIN}) called the critical inductance, to maintain continuous conduction mode with current minima just greater than zero, can be determined with the worst case operating conditions, as [16] [17].

$$I_O \geq I_{OB} = \frac{V_S * D * (1 - D)}{2 L f_S} \tag{1}$$

$$L_{MIN} \geq \frac{V_O * (1 - D)}{2 I_{OB} f_S} = \frac{V_O * (1 - \frac{V_O}{V_{S_{MAX}}})}{2 * (\frac{P_{O_{MIN}}}{V_O}) f_S} \tag{2}$$

where; I_O is the average value of load current, I_{OB} is the average value of load current at the boundary condition, $P_{O_{MIN}}$ is the minimum load power required, $V_{S_{MAX}}$ is the maximum value of input voltage, D is the duty-ratio, f_S is the switching frequency and V_O is the output voltage. When switch and inductor resistive drops are considered, L_{MIN} is

$$L_{MIN} \geq \frac{(V_O + I_O * R_L) * (1 - D)}{2 I_{OB} f_S}$$

$$= \frac{(V_O + I_O * R_L) * (1 - \frac{V_O}{V_{S_{MAX}}})}{2 * \frac{P_{O_{MIN}}}{V_O} f_S} \tag{3}$$

R_L indicate the leakage resistance of the inductor coil. The equivalent series resistance (ESR), equivalent series inductance (ESL), and capacitance (C) at switching frequencies determine the output voltage ripple. The value of filter capacitor required to limit output voltage ripple to the required level is given by

$$C \geq \frac{\Delta Q}{\Delta V_O} = \frac{\Delta I_L}{8 f_S \Delta V_O} \tag{4}$$

$$\Delta I_L = \frac{(V_S - V_O) * D}{L f_S} \tag{5}$$

where; ΔQ is the charge responsible for voltage ripple, ΔV_O is the peak to peak voltage ripple, and ΔI_L is the peak to peak ripple current through inductor. The equations assume that the entire ripple current of the inductor, flows through the capacitor and the ESR is negligible. Assuming that the capacitor is very large for inductor CCM operations, the ESR needed to limit the ripple to ΔV_O can be estimated as

$$ESR \leq \frac{\Delta V_O}{\Delta I_L} \tag{6}$$

As duty ratio swing is bound to lie within a narrow range as $\frac{V_{O_{MIN}}}{V_{S_{MAX}}} \leq D \leq \frac{V_{O_{MAX}}}{V_{S_{MIN}}}$ in a VRM, (1) can be rewritten as

$$I_{OB_1} = \frac{V_{O_{MIN}} (1 - \frac{V_{O_{MIN}}}{V_{S_{MAX}}})}{2 L f_S} \tag{7}$$

$$I_{OB_2} = \frac{V_{O_{MAX}} * (1 - \frac{V_{O_{MAX}}}{V_{S_{MIN}}})}{2 L f_S} \tag{8}$$

where I_{OB_1} and I_{OB_2} are the minimum values of load current necessary to establish inductor current continuity. In a VRM with widely varying output voltage demand, for a given minimum load power and fixed converter switching frequency, $I_{OB_2} \approx 2 I_{OB_1}$. To ensure entire load range is in CCM, a large value of inductance is required. It is preferable to use an inductor with smaller value to obtain good transient response. As a result there will be large current ripples within each converter. However these individual current ripples gets significantly reduced at the capacitor node when interleaved converter topologies are employed. Hence it is a standard practice in VRMs to use smaller values of inductance to achieve superior transient response. Typically VRM voltage conversion ratio is very small and hence OFF period is much longer compared to ON-time. As a result of using smaller inductance value, the circuit with bidirectional switch M2 will allow the current minimum to reach to below zero and filter capacitor tends to discharge. Inductor will store any energy released and once the MOSFET M2 is switched OFF and control MOSFET M1 is switched ON the reverse stored energy will get pumped back to the DC source via MOSFET M1. The Switch M1 is allowed to carry the positive current from the source only after the negative energy pumping process stops. It is to be noted that a component of source supplied energy flows to and fro i.e. between source and capacitor via circuit components and will act as a source of energy inefficiency within each converter, especially under light load conditions.

The only feasible alternative to restrict I_{OB_2} to lower values is to employ higher switching frequency. But use of higher frequency will increase the switching and driver losses of the converter and the operation tends to be inefficient at large load currents. It is therefore necessary to suitably bridge transient response and light load efficiency.

Converter operating with inductor current minimum reaching to values closer to zero is beneficial as it minimizes switching off loss in M2 and switching ON loss in M1. Also as the current reaches to below zero, there will be reduction in the ON-state losses and the heat produced in the switch, for the same current ripples. For a given inductor value (L=0.11μH) the current flowing through the inductor under lightly loaded condition for two different switching frequencies is shown in Fig. 2. The shaded areas show the current equivalent to the energy that is supplied back to the source during each cycle for different switching frequencies while converter is working in its worst case. The component of circulating energy spent in circuit is much larger compared to any energy that is saved through device loss reduction especially at smaller inductor values. From the above discussion we find that the overall circuit energy efficiency is significantly reduced as inductance value is lowered.

The solution then is to use higher inductor values, which will reduce the current ripples and hence the device losses. Fig. 3 shows the reduction in the circulating energy with increase in inductance value for worst case converter operation. However this is not a good solution as it deteriorates the overall transient response of the converter.

Another solution to reduce the circulating energy is to increase the switching frequency. Fig. 4 shows the reduction in circulating energy due to reduced current ripples with higher switching frequencies. In this approach there will be an increase in the frequency dependent losses and beyond an optimum switching frequency the efficiency starts to drop. Achieving good ripple cancellation becomes difficult when this approach is extended to multiphase interleaved topologies.

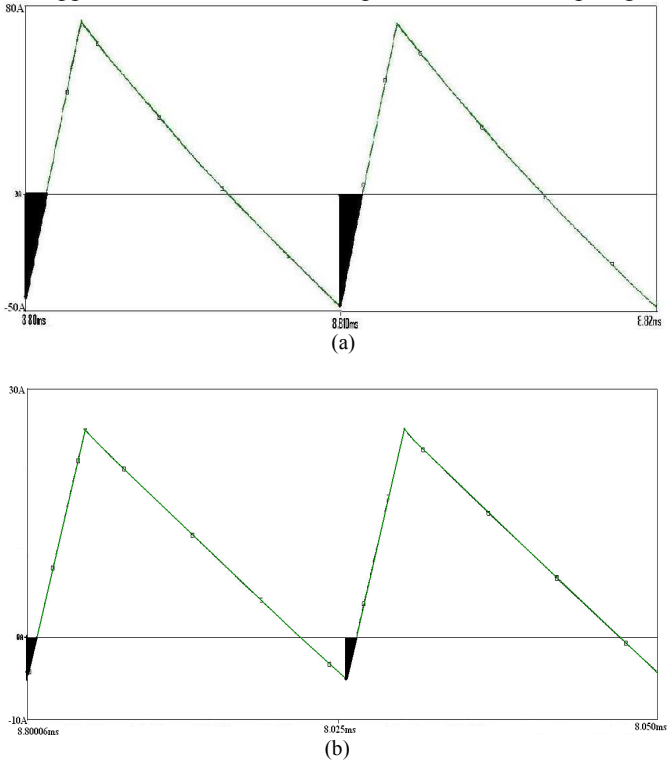

Fig. 2 Inductor current (a) f_S = 100 KHz (b) f_S = 400 KHz

Thus selecting a suitable value for I_{OB} is critical as it depends on source voltage, load voltage, inductor value and the switching frequency.

In VRMs, all of these parameters vary over a predefined range and each of them has an influence on the efficiency of the converter. When they are varied independently, circuit conduction losses either get directly affected or low duty ratio gets reflected as increased switching losses. Fig. 5 shows the efficiency band for the source voltage variation as a function of switching frequency for different inductors. Similarly Fig. 6 shows range of efficiency for the predefined load voltage range as a function of frequency for different inductors when the converter is lightly loaded. With smaller inductance, circuit losses are mainly due to circulating energy, where as with higher inductance, the ripple current and switching frequency dependent losses will determine the efficiency.

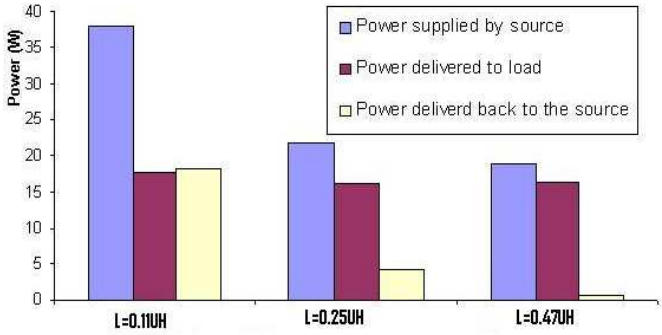

Fig. 3 Variation in circulating energy with filter inductance

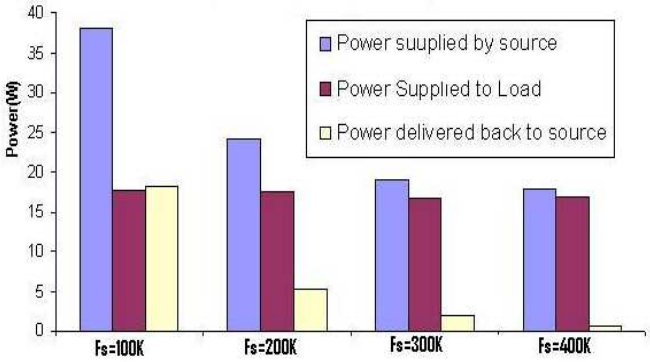

Fig. 4 Variation in circulating energy with switching frequency

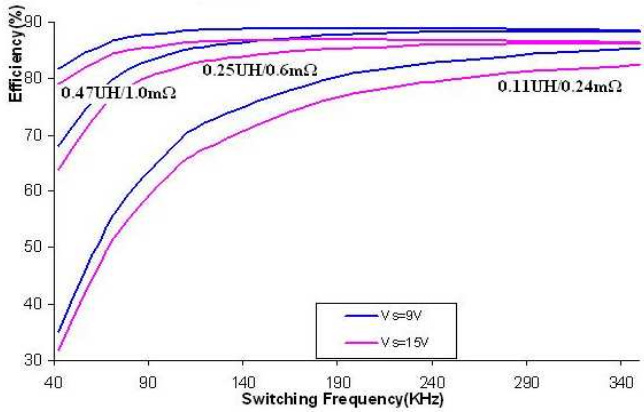

Fig. 5 Efficiency band for source voltage variation (V_O =1.6V, Io=10A)

Processor operating in its sleep mode is typically the worst case for the converter, while powered from battery. As sleep modes are likely for longer duration, any efficiency improvement will help saving significant amount of energy. Fig. 7 shows the influence of frequency on the efficiency for a typical case when the converter is working for processor in sleep mode on battery. Increase in switching frequency primarily helps in reducing circulating energy and thus reduces the ripple based losses for lower inductor values. However with larger inductor values it will only reduce ripple dependent losses. Fig. 8 shows the efficiency improvements while switching frequency is varied for converter working on the power adaptor when the processor is recovering from sleep mode to active mode operation, for different values of inductance. A close observation of Fig. 7 and Fig. 8 reveals that maximum efficiency point is obtained at lower frequency for higher inductance value. The maximum value of efficiency increases with inductor value as it reduces losses due to ripple current.

Hence a best solution is therefore to implement a variable switching frequency scheme where higher switching frequencies at light load ensures to maintain lower I_{OB} and lower frequency at higher load currents will ensure better efficiency for the converter supplying a variable load. This solution expects to regulate the current ripple suitably by adjusting switching frequency for given operating point. Though it appears to be similar to implementing a hysteresis control, it is different in nature by itself as hysteresis band is variable for the best efficiency as the operating point depends on source voltage, load voltage and load current. As a result of frequency variation, I_{OB} value in (7) and (8) are maintained quite close or may vary only over a small range. Fig. 9 and Fig. 10 show the influence of switching frequency on the converter efficiency for different load currents for a fixed inductance of 0.47µ. This indicates that the maximum efficiency of converter occurs at higher switching frequency for light loads and lower frequency for large load currents. The capacitor needed to limit the voltage ripple to within the tolerance band, is much smaller compared to that required to meet the transient response and hence the variable frequency approach shows its suitability in the context.

III. SIMULATION

A synchronous buck converter is designed to work with the following specifications: source voltage 9V to 15V to represent the case of laptops (in desktop systems the SMPS output is tightly regulated around 12V±5% and it is a subset of the case considered), load voltage 0.8V to 1.6V, load current per converter phase is 10A to 30A. Infineon BSC032NOS, MOSFETs are used for both control and freewheeling purpose. Coiltronics and Vishay make chip inductors were used for the study. The filter capacitance of 12.96mF is used to keep voltage ripple less than ±20mV for the lowest switching frequency. This is realized by using low ESR (Equivalent series resistance) KEMET make 6.3V rated tantalum capacitors. PSPICE circuit simulation environment of ORCAD® Capture 16.0 Version is used to simulate the circuit. The steady state efficiency of the converter is estimated using the results of each simulation run. The extreme operating points are then simulated with different switching frequencies to plot the steady state converter efficiency graphs given in the paper.

The variation in the converter efficiency as switching frequency is varied for different loads is shown in Fig. 9 and Fig. 10. It shows that higher switching frequency at light load will reduce the circulating energy to improve the efficiency of the converter. Similarly decreasing the switching frequency as load increases will help reducing the frequency dependent losses to achieve better efficiency. As the duty ratio is very small, the converter efficiency does not get affected much with source voltage variation. In our laptop simulation study we have considered wide variation of source voltage. Hence the efficiency changes due to the dynamic range of the source voltage can be ignored in the case of a VRM supplied from an SMPS as it is subject to much smaller range of voltage variations.

IV. CONCLUSION

The VRM design for high performance processor boards is an ever challenging area as its design constraints like higher steady state efficiency, tighter voltage regulation, smaller foot print and lower cost etc., gives limited options for the designer. This paper attempts to analyze the reason for low efficiency especially when the converter is lightly loaded. It also suggests a variable frequency approach wherein higher frequency at light load and lower frequency at larger load, as a cost effective solution to get best efficiency for all operating conditions. Moreover detailed analysis of the converter operation at its predefined boundary provides the knowledge about the range of switching frequency need to be used for given inductance value. However an insight into the converter design issues is necessary to exactly estimate the switching frequency to ensure best efficiency for all operating conditions. In spite of switching frequency being variable the capacitor value needed to limit the voltage ripple is very small as compared to that required to meet the transient response. Moreover as the input voltage variation does not affect the VRM efficiency significantly, the proposed solution can thus be employed for both desktop and laptop systems.

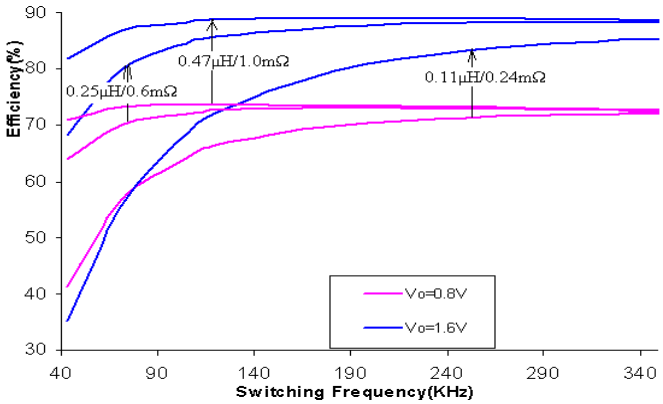

Fig. 6 Efficiency band for load voltage variation (Vs=9V, Io=10A)

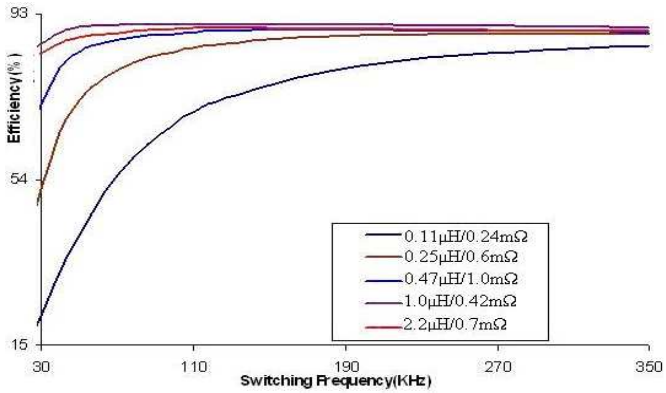

Fig. 7 Converter efficiency with different inductors (Boundary case V_S=9V, V_O=1.6V, I_O=10A)

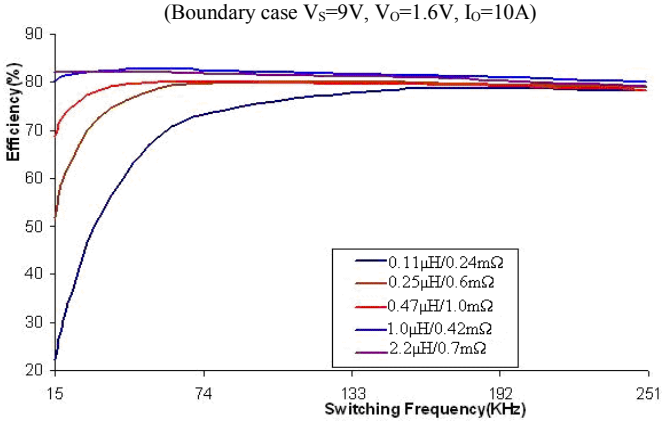

Fig. 8 Converter efficiency for different inductors (Boundary case V_S=15V, V_O=0.8V, I_O=30A)

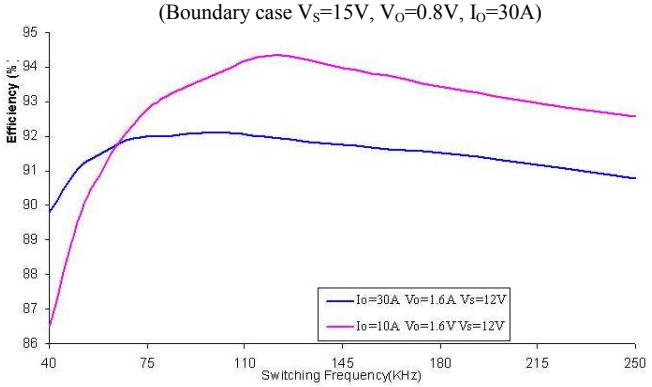

Fig. 9 Converter efficiency variation with load current

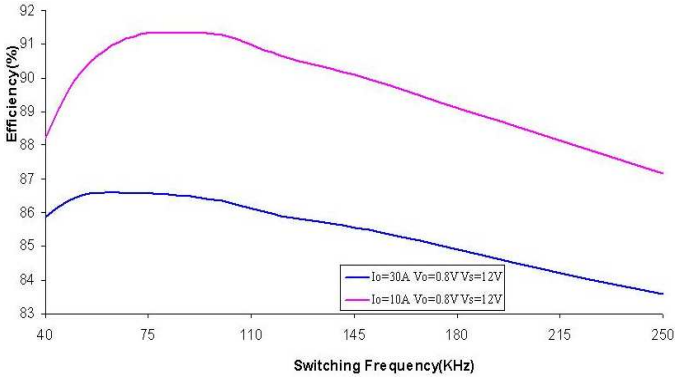

Fig. 10 Converter efficiency variation with load current

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