IMPLEMENTATION OF JPEG2000 STILL IMAGE CODEC ON BLACKFIN (ADSP – BF535) PROCESSOR

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Abstract: With increasing use of Multimedia in everyday life, there is a need not only for better image compression techniques which can be used in a wide range of applications but also for efficient implementation of these compression algorithms on power-efficient platforms. To cater to such needs several compression methodologies have been proposed and standardized. We have implemented, JPEG2000, an emerging standard for still image compression on the Analog Devices Blackfin Digital Signal Processor (DSP). Implementation of still-image compression on programmable DSPs offer several advantages like ease of changing the codec standard, improved value addition by customizing the codec to the target application, scalability in image sizes etc. This paper presents the implementation details of the JPEG2000 still image codec on ADSP-BF535 processor based Analog Devices EZ-kit Lite board, and the quality of the results obtained demonstrate the potential of the low-power Micro-Signal Architecture of Blackfin processor as a good choice for embedded multimedia applications.

Keywords: Image coding, JPEG, JPEG2000, Blackfin

1. Introduction

One of the most popular still-image compression standards is the JPEG standard. The encoding process involves Block DCT transform with Huffman coding. Despite the phenomenal success of the JPEG algorithm, its shortcomings become increasingly apparent as image compression is extended to more application domains like medical imaging, digital libraries, multimedia, internet and mobile. Some of the limitations are no target bit rate, no region of interest (ROI) coding, provides only single resolution and quality, and blocking artifacts at higher compression rates.

The emerging still-image compression standard, JPEG2000 (ISO 15444/ITU-T Recommendation T.800)[1] tries to overcome these limitations and provide subjective image quality performance superior to existing standards. It also offers a host of extra features like lossless and lossy compression, embedded lossy to lossless coding, progressive transmission by pixel accuracy and resolution, robustness to bit-errors, region of interest coding, content-based description etc. With JPEG2000, the *quality* of the resultant image depends upon the compressibility of the input image, while with JPEG, the *size* of the image depends on the compressibility of the input image.

The processor chosen by us for implementation of the JPEG2000 standard is the Analog Devices Blackfin processor, ADSP-BF535. It is a fixed point embedded media processor designed specifically to meet the computational demands & power constraints of todays embedded media applications. The architecture combines a dual MAC state-of-the-art signal processing engine, the advantages of a clean, orthogonal RISC-like microprocessor instruction set, and Single-Instruction, Multiple Data (SIMD) multimedia capabilities into a single instruction set architecture. Blackfin processors are designed in a low power and low voltage design methodology and feature dynamic power management, the ability to independently vary both the voltage and frequency of operation to significantly lower overall power consumption.

Sections 2 and 3 give an overview of the JPEG2000 standard and the architectural features of the target digital signal processor ADSP-BF535 respectively. The implementation issues are discussed in Section 4. In Section 5, we highlight the performance of the image codec on the ADSP-BF535 processor based Analog Devices EZ-kit Lite board. The results summarized in Section 6 demonstrate the potential of the Blackfin processor for implementing embedded multimedia applications.

2. Overview of JPEG 2000 codec

The fundamental building blocks of a JPEG2000 codec are shown in Fig. 1 [2],[3],[4][5]. The components are:

Preprocessing involves DC level shifting to achieve a dynamic range of values centered around zero.

Inter component Transform is to convert RGB planes to Luminance (Y) and Chrominance (Cb ,Cr) planes.

Intra component Transform is realized through Discrete Wavelet Transform (DWT). It decomposes the image into multiple resolution levels using a wavelet transform. For practical implementation, the lifting scheme is used to perform, in-place computation of DWT coefficients.

Quantization carried out on the transform coefficients using scalar quantization with a dead zone.

Tier-1 encoding with the subbands divided into code blocks. Embedded bit plane coding is the technique adopted for encoding the image. Each bit plane of each code block is passed through 3 coding passes namely: significant propagation pass, magnitude refinement pass and cleanup pass. A MQ encoder is used to code the bits.

Tier-2 encoding is essentially a process of organization of the bit-plane coding data from the Tier-1 coding into packets and output as code stream.

Rate control is achieved mainly by selection of a subset of coding passes to be included in the final code stream, with

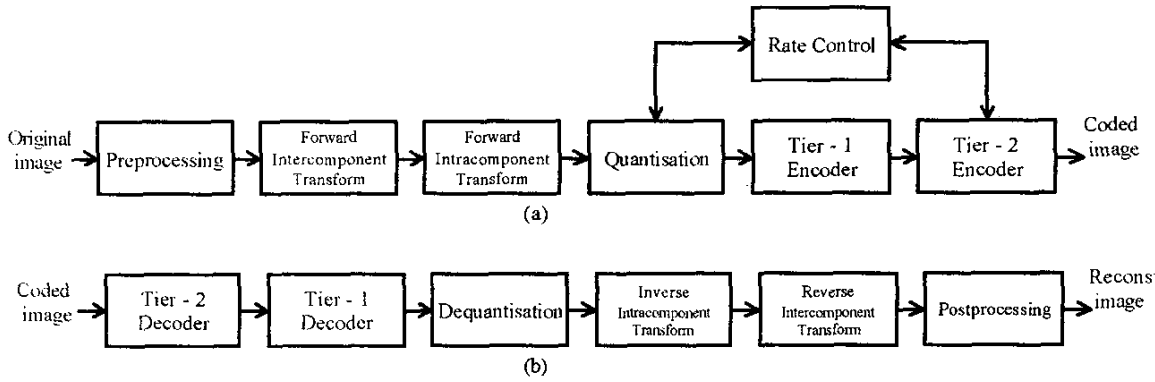

Fig. 1 JPEG2000 code structure (a) Encoder (b) Decoder

the knowledge of contribution of various coding passes and the distortion reduction due to their addition.

The basic encoding engine of JPEG2000 is based on EBCOT (Embedded Block Coding with Optimised Truncation of the embedded bit streams) algorithm. The inverse process is done at the decoder.

3. Blackfin processor ADSP-BF535

The ADSP-BF535 processor combines a 32-bit RISC-like instruction set and dual 16-bit multiply accumulate (MAC) signal processing functionality with an addressing capability extendable to nearly 4 Giga bytes. The functional diagram of the processor core is shown in Fig. 2 [6]. Its core architecture consists of, a Data Arithmetic Unit which includes two 16-bit Multiplier Accumulators (MACs), two 40-bit Arithmetic Logic Units (ALUs), four 8-bit video ALUs, and a single 40-bit barrel shifter. The two Data Address Generators (DAGs), support bit-reversed addressing and circular buffering. Other registers include, six 32-bit address pointer registers (P0-P5) for fetching operands, Index registers (I0-I3), modifier registers (M0-M3). Base registers (B0-B3) and Length registers (L0-L3). The ADSP-BF535 Blackfin processor contains a rich set of peripherals connected to the core via several high bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance.

The Analog Devices EZ-kit Lite board is based on the ADSP-BF535 Blackfin processor running at speeds up to 350MHz and consists of 308K Bytes of On-Chip Memory, SDRAM (16MB), flash memory (544kB) of external memory, and USB interface for data transfer between the host PC and the board at a rate of 150kB/s [7].

3. Implementation

The JPEG2000 still image codec has been implemented on ADSP-BF535 processor based Analog Devices EZ-kit Lite board running at 350MHz. The C code for JPEG2000 codec being used is available as part of open source JasPer transcoder (JasPer version: 1.700.2)[8] code. The Jasper source code has been optimized to suit the processor architecture. Analog Devices, Visual DSP++ v.3.5

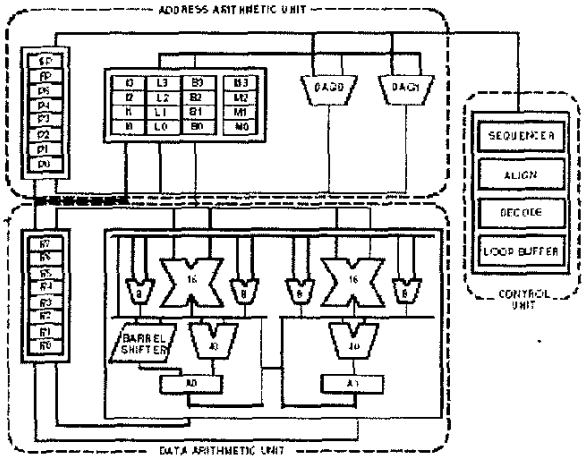

Fig. 2 Blackfin processor Core architecture

(VDSP++) was used as the code development and debug environment. A GUI was developed in Visual C++ (VC++) to interact with the EZ-kit Lite board via VDSP++ from the host PC.

3.1 Source Code Optimizations

The MQ encoder function calls have been suitably replaced by macros speeding up the process. DWT Lifting coefficients are declared as register variables for faster access. Look-up-tables (LUT) are being used for context variables instead of calculating for every bit plane. The task of finding context is made simpler by modifying context state information only when allocation becomes significant. Finding weighted mean square error (MSE) is essential for code stream organization and layering based on rate distortion. Conventional method is to decode the image with and without code block, compare and calculate the error, which is, an added overhead. An approximate method is used in our implementation to increase the speed. In this method, the MSE is incrementally changed whenever a location becomes significant. The algorithm used for rate allocation requires that in each iteration the passes which are to be included in the code stream have to be encoded as packets to find the final length of the code stream. Larger the number of iterations implies that larger is the time taken. If the

TABLE 1 CYCLE COMPLEXITY FOR VARIOUS JPEG2000 ENCODING BLOCKS

Major function	Total no. of Memory Copy operations	Add/ Sub operations	Logical operations	Multiply/ Divide operations	No. of Function calls	Total no. of operations
RCT	0.59	0.45	0.13	0	0	1.17
ICT	0.39	0.39	0.58	1.17	0	2.53
DWT	0.67	4.85	2.09	0.017	0.006	7.62
Quantization	0.49	0.39	0.89	0.78	0.002	2.57
EBCOT	8.36	1.54	1.24	0.015	0.34	11.50
Rate allocation	1.67	0.31	0.64	0.01	0.005	2.625
Total MOPS (million operations) for loss coding						**20.29**
Total MOPS (million operations) for lossy coding						**26.845**

length remains same in successive iterations and the deviation is marginal then the rate allocation can be truncated.

3.2 Codec Modifications

The encoder implementation required frequent file I/O operations for tiling of the input image, through the USB link between the PC host and the Blackfin EZ-kit Lite daughter board, which reduced the speed of execution. As these file I/O operations were being carried on by the DSP processor on-board, which is not optimized for such file operations, the estimation of processing time was difficult. To overcome this, a *3-point* solution was adopted, in which, all file I/O operations in the entire program were first bundled up into one single file I/O operation by transferring the entire image data from the host memory to the daughter board memory in the beginning of the encoder cycle. The file operations were replaced by equivalent memory accesses from the external SDRAM using buffers for input and output files. At the end of the encoder cycle the entire output data is transferred from the DSP board SDRAM to the host memory. The loading of the program, buffer initialization (only one occurrence), loading of the image to the EZ-kit Lite memory and transfer of compressed data back to the host have been carried out through a plug-in built using VC++, which interacts with the VDSP++ platform by means of a set of Application Programming Interfaces (APIs). Provisions for debugging have also been provided in the plug-in. This GUI also initiates the encoding and decoding operation on the EZ-kit Lite board. Also, sufficient memory heap for dynamic memory allocation has been provided and some of the sparsely used program segments have been put into external memory while frequently used ones into internal program memory.

4. Performance Analysis

Performance analysis of the JPEG2000 codec has been performed with the standard Lena test (color with RGB components) image of size 256x256 pixels.

4.1 Encoding process

The encoding process consists of conversion of a bitmap (BMP) image to JPEG2000 (JP2) image. It comprises of two stages, BMP image decoding process followed by JP2 encoding process. BMP image decoding is essentially a process of extracting the RGB values from BMP image data and storing in DSP board memory. The JP2 encoding process follows the structure described in Section 2.

4.2 Operational Complexity

The total cycle complexity of the encoder for the test image (256x256) including all sub modules is approximately 26 MOPS (Million Operations) in case of lossy coding while it reduces to 20 MOPS for lossless coding. The difference is due to the rate allocation process which is responsible for deciding which of the coding passes should be included in the final coded bit plane data. It is also observed that the computational complexity of JPEG2000 standard is about three times that of JPEG compression standard. This is mainly due to the large analytical complexity involved in DWT (7.62 MOPS) and huge operational complexity involved in EBCOT (11.49 MOPS). The MOPS consumed by each block is shown in the Table 1.

4.3 Cycle Complexity

Percentage Cycle count for BMP decoding process is 6.54% while the Percentage Cycle count for JP2 encoding process is 93.42%. The cycle complexity for the various sub blocks of the JPEG2000 codec are given in Table 2. The coding passes namely the significance, magnitude refinement and cleanup take up the major portion of the cycles consumed.

4.4 Decoding process

The decoding process consists of JP2 decoding followed by BMP encoding. The total cycle complexity of the decoder for the test image (256x256) is approximately 22 MOPS. The Percentage Cycle count for JP2 decoding is 88.35% and that for BMP encode process is 11.18%. The inverse DWT module has been hand coded in assembly exploiting the parallelism and vector operations available in ADSP BF-535 to optimize performance.

4.5 PSNR Calculation

For the standard Lena test image of 256x256 pixels, the PSNR (Peak Signal to Noise Ratio) calculation has been done with individual components namely RGB contri-

TABLE 2. PERCENTAGE CYCLE COUNT FOR ENCODER

Sub processes	Functions	% cycle count
Preprocessing	Tile creation	3.677
	DC shift	0.564
Inter component transform	RCT	0.518
Intra component transform	Tree filtering	4.216
Quantization		0.827
Tier-1 coding	LUT initialization	0.166
	Significant pass	27.285
	Refinement pass	13.328
	Cleanup pass	25.978
Tier-2 coding	Header encoding	0.319
	Tag tree encoding	1.85
Rate allocation		11.952

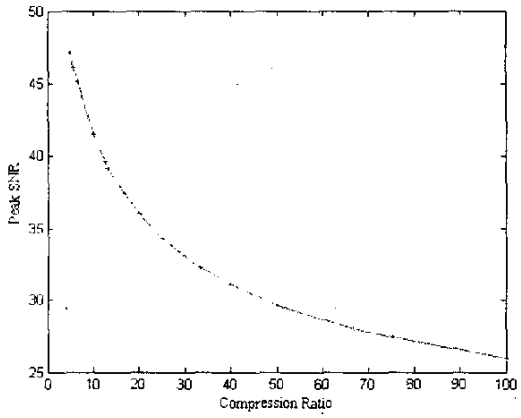

Fig. 3 PSNR vs Compression Ratio (Lena image 256x256)

butions combined to form that of Luminance using the RGB to Y (luminance) conversion matrix. A plot visualizing the objective quality of the image codec is shown in Fig. 3.

4.6 Visual Quality

For a given compression ratio, JPEG2000 gives much better visual quality than the JPEG standard as illustrated in Fig. 4. It is to be observed that at higher compression ratios JPEG images suffer from problem of blocking artifacts, due to block processing. In other words, visual quality deteriorates at a slower rate in JPEG2000 at higher compression ratios compared to JPEG or for a given visual quality; JPEG2000 provides much higher compression than that can be obtained with JPEG.

5. Results

The JPEG2000 codec was successfully implemented on Analog Devices Blackfin processor (ADSP BF-535) and results obtained are promising. The performance of the

bmp image **jpeg image** **jp2 image**

Compression ratio=71

Fig. 4 Comparison of original bmp with JPEG and JPEG2000 compressed images

codec demonstrates the potential of the low-power Micro-Signal Architecture of Blackfin processor as a good choice for embedded multimedia applications. Apart from giving good quality compression, the enhanced features of the codec make it the best choice for handheld multimedia devices. We are currently improving the efficiency of the implementation by hand coding time critical functions in assembly exploiting the architectural features of the processor like dual MAC, efficiently pipelined core and on-chip cache memory.

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